AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A process for controlling a PMC memory component, comprising ~~the steps~~:

[[-]] ~~Sending~~ sending out a signal to select one of several possible modes for the PMC memory component; and

[[-]] ~~Operating~~ operating the PMC memory component in accordance with the specific mode selected by the signal, wherein depending on the specific mode selected the PMC memory component is brought into states of different storage permanence by correspondingly selecting a current intensity and/or a duration of a programming pulse, and/or a number of programming pulses.

2. (Currently amended) The process of claim 1, further~~additionally~~ comprising ~~the step:~~

[[-]] ~~Writing of~~ writing data into the memory component in accordance with the specific mode selected by the signal.

3. (Currently amended) The process of claim 2, whereby one of the ~~possible~~ modes is a soft writing mode.

4. (Currently amended) The process of claim 2, whereby one of the ~~possible~~ modes is a non-volatile writing mode.

5. (Currently amended) The process of claim 2, whereby one of the ~~possible~~ modes is a hard writing mode.

6. (Currently amended) The process of claim 2, whereby for the writing of data into the memory component, ~~depending on the selected mode the~~ a current intensity, ~~and/or the~~ a duration of a programming pulse is adapted, and/or ~~the~~ a number of programming pulses.

7. (Original) The process of claim 1, whereby the memory component comprises PMC memory cells.

8. (Original) The process of claim 1, whereby the signal is sent out over one or several separate mode selection lines.

9. (Original) The process of claim 1, whereby the signal is sent out over the same line as actual data to be stored in the memory component.

10. (Currently amended) The process of claim 9, whereby the signal is sent out over ~~said~~ the line by use of memory mode selection bits, ~~said~~ the bits being followed by bits carrying the data to be stored in the memory component.

11. (Currently amended) A memory system, comprising:

[[-]] a memory component[[,]]; and

[[-]] a controller~~, the controller being~~ adapted to operate the memory component in at least one of several ~~possible~~ modes.

12. (Currently amended) The system of claim 11, whereby one of the ~~possible~~ modes is a soft writing mode.

13. (Currently amended) The system of claim 11, whereby one of the ~~possible~~ modes is a non-volatile writing mode.

14. (Currently amended) The system of claim 11, whereby one of the ~~possible~~ modes is a hard writing mode.

15. (Original) The system of claim 11, whereby the memory component comprises PMC memory cells.